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FDC37C93x Tips: Enabling Gate A20 and Keyboard Reset and General Purpose I/O Options

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GATE A20 AND KEYBOARD RESET

Due to the high feature integration level and advanced options available in SMSC's Ultra I/O devices, such as the SMSC FDC37C93x, and future I/O controllers, certain legacy functions may require design modifications from prior designs. Specifically detailed below are the GATE A20 and KEYBOARD RESET functions.

Required design modifications are, in this case, due to integration and should be limited to system BIOS. In the past, the keyboard controller has been a stand-alone 8042 microcontroller with fixed pinouts and options. With the advent of SMSC's advanced I/O controllers, which integrate this function, fixed pinouts and options no longer hold true. SMSC has incorporated programmable options within our advanced I/O controllers that allow legacy support, if required. If legacy support is not required, these pins may be used to support advanced features.

Detailed below are the BIOS additions required to enable the SMSC FDC37C93x to support the legacy GATE A20 and KEYBOARD RESET functions. Definition, explanation and history of these signals and functions is also presented.

GATE A20

The following paragraphs detail the GATE A20 issues listed below.

- What is GATE A20?
- What is the source of GATE A20?
- How is it manipulated?
- Why does it exist?
- Why do we need GATE A20?

What is GATE A20?

A20 is, as the name implies, is system address line 20.

GATE A20 is the name of the signal, that when gated with A20, will either enable or disable it. When enabled, addresses higher then A19, i.e. A20, generated by the CPU will be 'presented' to the system. 'Presented' generally means to access memory. A20 is enabled when GATE A20 is a one. This allows memory access to the region 0x100000 to 0x10FFFF hex. This memory area is commonly termed High Memory Area (HMA). When disabled, addresses above A19 will not be 'presented' to the system. A20 is disabled when GATE A20 is low. This forces an address 'wrap' above A19.

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What is the source of GATE A20?

In legacy systems, this signal was sourced from the keyboard controller (8042 microcontroller). The keyboard controller was one of the only sources of 'free' general purpose I/O. The 8042 microcontroller has two general purpose I/O ports, P1 and P2. Port two, bit one (P2.1) is assigned the GATE A20 function.

SMSC's advanced I/O controllers integrate the keyboard controller. If legacy keyboard controller GATE A20 support is required, this document details implementation with SMSC's advanced I/O controllers.

How is it manipulated?

Keyboard controller port control is accomplished via CPU to keyboard controller command passing. These commands are written to the command register at I/O address 0x060. The command for write Port 2 is D1h. The next byte specifies the port value.

Why does it exist?

The GATE A20 function is a left over from the 8088 and 80286 days. Certain programmers realized that, when using the 8088, they could take advantage of the 'wrap feature' by addressing above A19. When the 80286 was introduced, this 'feature' no longer worked. This was the result of segmentation and an increased number of address lines. Even though the 80286 running in 'REAL' mode truncates the segment register to 16 bits, like the 8088, it can actually end up addressing more that 1 megabyte of memory and driving A20 high.

In order to inhibit driving A20 high in 80286 and the newer 80386 and 80486 processors, the signal GATE A20 was created. When GATE A20 is enabled, an 8088 environment is assured. Software using the 'wrap feature' is then compatible with all systems.

Why do we need GATE A20?

Maybe you do not. GATE A20 support is only required if support for those 8088 programs which used the 'wrap feature' is desired.

Additionally, keyboard controller support of GATE A20 yields slow response. If support for 'FAST GATE A20' exists elsewhere in your system design, these FDC37C93x I/O pins may be used for implementing advanced features such as power management support.

KEYBOARD RESET

The following paragraphs detail the KEYBOARD RESET issues listed below.

- What is KEYBOARD RESET?
- What is the source of KEYBOARD RESET?
- How is it manipulated?
- Why does it exist?
- Why do we need KEYBOARD RESET?

What is KEYBOARD RESET?

KEYBOARD RESET initiates a 'soft boot'. Its function is to reset the host CPU only.

What is the source of KEYBOARD RESET?

The source of KEYBOARD RESET is the 8042 P2.0.

How is KEYBOARD RESET manipulated?

KEYBOARD RESET is toggled by sending a 'port output' command to the 8042.

Why does KEYBOARD RESET exist?

Keyboard reset is usually used to switch from protected to real mode.

Why do we need KEYBOARD RESET?

Again, you may not. The requirements are system-specific. This signal is often replaced by FAST RESET or ALT CPU RESET. FAST RESET or ALT CPU RESET are generally integrated into 'newer' core chipsets. In the 8042's case, the delay from command to actual reset can be hundreds of microseconds. Using FAST RESET, usually located at I/O 92h, delay times are as low as seven microseconds.

CONFIGURING THE FDC37C93Xx TO PROVIDE GATE A20 AND KEYBOARD RESET

Note:

- All General Purpose I/O defaults to INPUTS and NON-INVERT
- General Purpose I/O is LD8 (Logical Device 8)
- You must be in the Configuration Mode to perform any operations shown below

GP25 (8042 P2.1) is GATE A20

This is pin number 110 on the FDC37C93x and the FDC37C93xFR

LD8		
Write 0 to Bit 0 of reg EDh	rem :	Makes GP25 an output 0 = Output 1 = Input
LD8		
Write X to Bit 1 of reg EDh	rem :	X = Desired Polarity 0 = Non-inverting 1 = Inverting
LD8		
Write 1 to Bit 3 of reg EDh	rem :	Selects Alt Function GATE A20 for GP25

GP20 (8042 P2.0) is KEYBOARD RESET

This is pin number 105 on the FDC37C93x and the FDC37C93xFR

LD8		
Write 0 to Bit 0 of reg E8h	rem :	Makes GP20 an output 0 = Output 1 = Input
LD8		
Write X to Bit 1 of reg E8h	rem :	X = Desired Polarity 0 = Non-inverting 1 = Inverting
LD8		
Write 1 to Bit 4 of reg E8h	rem :	Selects Alt Function KBDRST for GP20
Finally, you must ENABLE LD8		Write 01h to Register 30h

FDC37C93xFR

Additional General Purpose I/O (GPIO) multiplexing options are available with the FDC37C93xFR. They are detailed below, as related to GATE A20 (pin number 110) and KEYBOARD RESET (pin number 105). Please refer to SMSC's FDC37C93xFR data sheet for additional information.

Pin Number	Original Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Default	Index Register	GPI/O
105	GPI/O	IDE2 Output Enable	8042 P2.0	-	Input	GP2	GP20
110	GPI/O	8042 P2.1	-	-	Input	GP2	GP25