DE520 Driver Development Information

Fast EtherWORKS PMC/PCI Adapter

OEM Business Group

Digital Equipment Corporation
Maynard, Massachusetts

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Contents

1.0 Document Overview

This document contains information on the Fast EtherWORKS PMC/PCI Adapter module, part number DE520-Ax, to assist in the development or porting of device drivers.

In addition the following three manuals should be available.

- From the OEM Business Group

  Fast EtherWORKS/PMC User Information, Part Number EK-DE520-IG

- From DIGITAL Semiconductor, on the LAN Controller

  DECchip 21140 PCI Fast Ethernet LAN Hardware Reference Manual, Part Number EC-QC0CA-TE

  DECchip 21140 PCI Fast Ethernet LAN Data Sheet, Part Number EC-QC0BB-TE

Hardcopies of the manuals can be obtained by calling DECdirect at 1-800-DIGITAL or writing

Digital Equipment Corporation
P.O. Box CS2008
Nashua, NH 03061

PostScript versions are available via the world wide web at

`http://www.digital.com:80/info/semiconductor/.`

2.0 General Purpose Register (GEP)

The following defines the General Purpose Register (GEP), CSR12, for the DE520-XA module. Refer to section 3.2.2.11 of the *21140 Hardware Reference Manual* for port configuration information.

GEP Bit	**Input/Output**	**Name**	**Function**
7	Input	Link Pass	10BASE-T Receive Link Status 0 = Link Pass 1 = No Link Pass
6	Input	SYM Link	100BASE-TX Receive Link Status 0 = Link ON 1 = Link OFF
5	Input	Signal Detect	Don't Care
4	Input	Not Used	Don't Care
3	Output	FDX Enable	Select Mode 0 = FDX Enable 1 = CSMA/CD Mode
2	Output	Transceiver Chip Loopback	Loopback Mode 0 = No Loopback 1 = Loopback Enable
1	Output	Force Activity LED ON	Activity LED Mode 0 = No Force LED ON 1 = Force LED ON
0	Output	Speed Select	Select Transmit Switch 0 = Select 10 1 = Select 100

Notes:

1. 10 Mbps and 100 Mbps modes are selected by CRS6. Refer to the DC21140 spec.
2. On initialization, select the 10 Mbps mode while performing 10/100 autosensing function.
3. In 100 Mbps mode, the 10BASE-T Link Pass Bit (GEP Bit 7) is not valid.

3.0 DIGITAL DE520 SROM Data V1.0

Byte Offset	Data	Description
00	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Reserved Field (All Zeros)
18	01	SROM Format Version
19	01	Adapter Count
20	XX XX XX XX XX XX	IEEE Network Address
26	00	Adapter 0 Device Number
27	41 00	Adapter 0 Leaf Offset
29	44 45 35 30 30 2D 58 41	Adapter Name 'DE520-AX'
37	11 01	Status (ABG Info)
39	YY YY YY YY YY YY YY YY YY YY	Serial Number in ASCII Format
49	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Reserved for ABG Future Use
65	00 08	Selected Connection Type - Autosense
67	0F	General Purpose Control
68	04	Media Count
69 (Media#1)	00	Media Code - TP (10Mb)
70	08	GP Port Data
71	9E 00	Command
73 (Media#2)	03	Media Code - SYM_SCR (100MBaseTX)
74	09	GP Port Data
75	ED 00	Command
77 (Media#3)	05	Media Code - SYM_SCR Full Duplex
78	01	GP Port Data
79	ED 00	Command
81 (Media#4)	04	Media Code - TP Full Duplex
82	00	GP Port Data
83	9E 00	Command
85	00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00	Unused
126	ZZ ZZ	2 LSBs of CRC 32

XX = IEEE Address Bytes
YY = Serial Number
ZZ = CRC32

4.0 Tulip FasterNet Driver Unification

The following tables highlight the modifications needed to port a 21040 driver to a 21140 driver.

4.1 Register Value Differences

The list below summarizes the FasterNet/Tulip programmable differences from the port-driver point of view.

CSR	Bit	Name	FasterNet Modification
5	10	AT	Not applicable. Read always as zero.
	11	GTE	Functional difference. Used by the 21140 to indicate that the gp timer expired.
	12	LNF	Not applicable. Read always as zero.
6	10:11	OM	The same values remain, but the table which listed the operation mode in combination with CSR14 is no longer applicable.
	14:15	TR	The actual interpreted threshold values were changed with respect to FIFO size difference. However bits 14:15 still have the same functional meaning from the driver point of view. If CSR6.22 == 1, then values are the same as 21040.
	18	PS	This bit selects between Fast/Normal Ethernet mode. On reset, this bit is set to zero, which means Normal Ethernet mode (EXT_SIA port is active).
	19	HBD	Heart Beat disable mode. This bit should be set to one for Normal Ethernet mode and zero for Fast Ethernet mode.
	21	SF	Full packet. When set a transmission is started only when a full packet resides in the FIFO regardless of the values specified in CSR6<TR>.
	22	TTM	MII Rate. This bit selects between MII/SYM 100MBps data rate and MII/SYM 10MBps data rate. It also selects between the 100MBps and 10MBps transmit threshold value when operating in MII/SYM mode.
	23	PCS	PCS Mode. When set, the PCS functions become active and the MII/SYM port operates in symbol mode.
	24	SCR	Scrambler Mode. When set, the scrambler function becomes active and the MII/SYM port transmits and receives scrambled symbols.
	25	MB1	Must be programmed to 1.
	28:26		Must be 0.
7	10	ATM	Not applicable.
	11	GPT	Functional difference. Used by the 21140 to enable gp timer interrupts.
	12	LFM	Not applicable.
12	all	General purpose pins register in FasterNet pass2. (SIA status register in Tulip)	
13	all	Not implemented. Read as FFFFFFFFh	

CSR	Bit	Name	FasterNet Modification
14	all	Not implemented. Read as FFFFFFFFh	
15	8	MBZ	Must be 0.
	9	FUSQ	Not implemented.
	10	FLF	Not implemented.
	12	DPST	Not implemented.
	13	FRL	Not implemented.
CFID	31:16	Updated device ID number. 0x00091011.	
CFRV	3:0	Updated configuration revision number.	
	7:4	Updated step number.	

4.2. Descriptors Differences

The list below summarizes the FasterNet/Tulip programmable differences from the Descriptor-driver point of view.

Descriptor	Bit	Name	FasterNet Modification
RDES0	1	CE	Is set to indicate that a CRC error occured during frame reception, or when mii_err asserts.
RDES0	3	MB1	Always high.
RDES0	15	ES	Error summary now includes MII_ERR assertion as well.

5.0 SROM CRC Calculation Algorithm

```
unsigned short CalcSromCrc(unsigned char *SromData);
    #define DATA-LEN   126   //1024 bits SROM
    struct{
      unsigned char SromData[DATA_LEN];
      unsigned short SromCrc;
      } Srom;
    main()
    {
    Srom.SromCRC = CalcSromCrc(&Srom.SromData);
    }
    unsigned short CalcSromCrc(unsigned char *SromData)
    {
    #define POLY 0x04C11DB6L
      unsigned long crc = 0xFFFFFFFF;
      unsigned long FlippedCrc = 0;
      unsigned char CurrentByte;
      unsigned Index;
      unsigned Bit;
      unsigned Msb;
      init i;
    for (index = 0; Index < DATA_LEN; Index++)
    {
      CurrentByte = SromData[Index];
      for (Bit = 0; Bit < 8; Bit ++)
      {
            Msb = (crc >> 31) & 1;
            crc << 1;
            if (Msb ^ (CurrentByte & 1))
            {
               crc ^ = POLY;
               crc != 0x00000001;
            }
            CurrentByte >>= 1;
      }
    }
    for (i=0; i < 32; i++)
    {
      FlippedCRC <<= 1;
      Bit = crc & 1;
      crc >>= 1;
      FlippedCRC += Bit;
    }
    crc = FlippedCRC ^ 0xFFFFFFFF;
    return (crc & 0xFFFF);
    }
```

6.0 21140-AA Errata

CONTENTS

This section contains Errata for the DECchip 21140 Rev B (Pass1.1) chip. The Errata sheets describe anomaly associated with this revision of the 21140 and offer workarounds, possible, to allow system designers and driver developers to use the DECchip 21140 successfully.

Throughout this section, the *DECchip 21140 Data Sheet* (document number EC-QC0BB-TE) is referred to as the Data Sheet; the *DECchip 21140 Hardware Reference Manual* (document number EC-QC0CA-TE) is referred to as the Hardware Reference Manual.

Errata Revision 1.2 10/Apr/1995

6.1. Operation in Systems Running PCI at 25MHz

Background

The DECchip 21140 Data Sheet specifies its PCI bus clock operating range to be 25MHz to 33MHz (Data Sheet page 2).

Problem

In some systems the PCI clock frequency, although stated to be 25MHz, may be fractionally faster or slower than 25MHz. Another clock which is supplied to the 21140, the MII/SYM_TCLK, is 25MHz controlled by a crystal. The crystal controlled MII/SYM_TCLK will typically be accurate approximately 100ppm.

When the frequency of the PCI clock is lower than the frequency of the MII/SYM_TCLK, there is a chance that an excessive number of packets will be transmitted with CRC errors, or that the 21140 will report a transmit underflow condition. This anomaly is related only to 100Mbps transmission in conjunction with PCI operation at 25MHz. It does not affect the more common PCI operating frequencies of 30MHz or 33MHz.

Implications

The 21140 may not function properly in some systems that specify that the PCI bus is operated at 25MHz.

Workaround

The 21140 can be used in systems where the PCI frequency is constantly higher than the frequency of the MII/SYM_TCLK, which is nominally a very accurate 25MHz. For systems that have a clock frequency fractionally slower than the MII/SYM_TCLK, an enhancement to the design will be required for the 21140 to operate in its 100Mbps modes. This enhancement is planned for the next design revision.

6.2. Efficiency of Capture Effect Algorithm

Background

The Capture Effect feature is enabled setting CSR6 bit 17. In this mode, the DECchip 21140 selectively chooses between two types of backoff algorithms in order to prevent the capture effect situation from occurring. The capture effect is described in more detail in section 6.6 of the Hardware Reference Manual.

This mechanism is not part of the IEEE 802.3 standard but works in conjunction with the standard protocol.

Problem

When working with an MAU that returns heartbeat signals, the Capture Effect Algorithm may not work to its best efficiency as indicated in the Hardware Reference Manual. The loss of efficiency occurs when only one good transmission succeeds without collision following the backoff 2 or the backoff 0 stages.

The Capture Effect Algorithm will work to its best efficiency following the backoff 2 or the backoff 0 stages only if at least two packets are transmitted successfully.

Implications

Enabling the Capture Effect mode on the 21140 does not eliminate the problematic Capture Effect phenomena. Instead it only reduces its effect.

Workaround

The MAU should be configured with the heartbeat signal disabled if the Capture Effect feature is used.

A correction of the Capture Effect algorithm is planned for the next design revision.

6.3. Hash/Perfect Filtering Mode

Background

The DECchip 21140 offers several schemes to filter incoming packets based upon their Ethernet addresses. In most cases, the perfect filtering mode is used to filter up to 16 addresses. In the Hash/Perfect filtering mode, when more than 16 addresses are required, the 21140 performs imperfect address filtering of multicast incoming frames according to the hash table specified in the setup frame. The physical addresses are perfect filtered by comparing them to a single address, generally the station address. The filtering modes are described in Table 4-8 of the Hardware Reference Manual.

Problem

When operating in the Hash/Perfect filtering mode, the 21140 does not filter the single physical address correctly.

Implications

The anomaly with the Hash/Perfect filtering mode is worked around in drivers for the DECchip 21140 developed by DIGITAL.

In non DIGITAL developed drivers, the 21140 cannot be operated in Hash/Perfect filtering mode if physical addresses need to be filtered. One of the workarounds can be implemented to avoid this anomaly.

Workaround

There are two software alternatives which can be applied:

1. Use the perfect filtering mode for filtering physical address and set the "All Multicast" mode for receiving all the multicast addresses.
2. Use the Hash Only filtering mode for both physical and multicast addresses. The physical address should also be filtered by software.

6.4. Behavior of MII_MDIO Signal Following Reset

Background

The MII_MDIO signal (pin 105) is an input/output signal that transfers control information and status between the PHY and the DECchip 21140 when the MII port is used.

Problem

Following reset, the MII_MDIO signal is driven to zero.

Implications

This behavior does not comply with the MII standard IEEE 802.3u.

Workaround

The anomaly is only relevant before the driver has initialized the 21140. The driver controls the operation mode of the MII port. Setting the MII operation mode to read will place the MII_MDIO signal in tri-state. The MII operation mode is described on pages 3-41 and 3-42 of the Hardware Reference Manual.

In the next design revision, it is planned to modify the MII_MDIO signal to tri-state following reset.

6.5. SYM_LINK Signal Relationship to Descrambler

Background

The SYM_LINK signal is an output from the DECchip 21140. SYM_LINK gives the status of the 100Mbps line when using the internal PCS decoder. If the internal descrambler is enabled (by setting CSR6 bit 24), the SYM_LINK signal reflects whether the descrambler is locked to the incoming scrambled data stream (page 2-9 of the Hardware Reference Manual).

Problem

The assertion of the SYM_LINK signal does not reflect the scrambler lock condition when the scrambler function is enabled. The SYM_LINK assertion is related only to the signal detect (SD) input. The SYM_LINK signal will assert 330μs after the 21140 has detected that the SD input is asserted.

If the descrambler loses lock of the scrambled data stream and SD remains asserted, SYM_LINK will deassert for 330μs and then reassert independent of the scrambler lock status.

Implications

The SYM_LINK signal cannot be used for detection of 100Base-TX scrambled data. Instead, the SYM_LINK signal will reflect only the value of the link status as defined in the IEEE 802.3u standard. In situations where the scrambler is enabled, the SYM_LINK behavior may complicate the implementation of autosensing on the 21140.

Workaround

Various algorithms are presently being investigated to permit autosensing with 100Base-TX scrambled data.

In the next design revision, it is planned to modify the SYM_LINK output signal to also indicate the descrambler lock status when the descrambler is enabled.

6.6. Behavior of SYM_LINK Following Link Failure

Background

The SYM_LINK signal from the DECchip 21140 chip gives the status of the 100Mbps line when using the internal PCS decoder. The SYM_LINK signal is asserted 330µs after the assertion of the signal detect (SD) input signal.

Problem

If one or more transmits are pending at the time that SYM_LINK needs to be reasserted, the SYM_LINK reassertion (which reflects the internal link status) is delayed. This avoids transmission of a truncated packet. The SYM_LINK signal may remain deasserted as long as there are packets awaiting transmission.

Implications

This anomaly with the delayed SYM_LINK assertion is worked around in drivers for the DECchip 21140 developed by DIGITAL.

In non-DIGITAL developed drivers, if the work-around is not implemented, some packets which were intended to be transmitted may not reach the line and some packets intended to be received may be lost.

Workaround

This issue can be worked around in software. The SYM_LINK signal can be routed to the GEP port and polled by the driver. If the signal is deasserted, the driver should stop the transmit process and re-enable it after 500µs or after SYM_LINK reassertion.

In the next design revision, it is planned to modify the SYM_LINK output signal to reassert 330µs after re-establishment of a link, independent of whether there are packets awaiting transmission.

7.0 21140-AB Errata

CONTENTS

This section contains Errata for the DIGITAL Semiconductor 21140 Revision 1.2 chip (also known as DC1010 Revision C). The Errata sheets describe problems associated with this chip or its documentation and offer workarounds which allow system designers and driver developers to use the 21140 successfully.

Throughout this section, the *DIGITAL Semiconductor 21140 Hardware Reference Manual* is referred to as the Hardware Reference Manual.

Errata Revision 1.2 4/Jan/1996

7.1. Hash/Perfect Filtering Mode

Background

The DIGITAL Semiconductor 21140 offers several schemes to filter incoming packets based on their Ethernet addresses. In most cases, the perfect filtering mode is used to filter up to 16 addresses. In the Hash/Perfect filtering mode, when more than 16 addresses are required the 21140 performs imperfect address filtering of multicast incoming frames according to the hash table specified in the setup frame. The physical addresses are perfect filtered by comparing them to a single address, generally the station address. The filtering modes are described in Table 4-8 of the Hardware Reference Manual.

Problem

When operating in the Hash/Perfect filtering mode, the 21140 does not filter the single physical address correctly.

Implications

The anomaly with the Hash/Perfect filtering mode is worked around in drivers for the 21140 developed by DIGITAL Semiconductor.

In non DIGITAL Semiconductor developed drivers, the 21140 cannot be operated in Hash/Perfect filtering mode if physical addresses need to be filtered. One of the workarounds can be implemented to avoid this anomaly.

Workaround

There are two software alternatives which can be applied:

1. Use the perfect filtering mode for filtering physical address and set the "All Multicast" mode for receiving all the multicast addresses.
2. Use the Hash Only filtering mode for both physical and multicast addresses. The physical address should also be filtered by software.

8.0 21140A-AC Errata

CONTENTS

This section contains Errata for the DIGITAL Semiconductor 21140A PCI Fast Ethernet Controller. The 21140A device revision which is affected by this errata is identified as order number 21140-AC, in software as CFRV<7:0>=20(hex), and is also labeled as DC1036DA.

The Errata sheets describe problems associated with this chip or its documentation and offer workarounds which allow system designers and driver developers to use the 21140 successfully.

Throughout this document, the DIGITAL Semiconductor 21140A Fast Ethernet Controller is referred to as the 21140A; the *DIGITAL Semiconductor 21140A Hardware Reference Manual* (order number EC-QN7NC-TE) is referred to as the Hardware Reference Manual; and the *DIGITAL Semiconductor 21140A Data Sheet* (order number EC-QN7PB-TE) is referred to as the Data Sheet.

Errata Revision 1.4 6/Jun/1996

8.1. Operation in Systems Operating at PCI Frequencies Between 20-25MHz

Background

The DECchip 21140A Data Sheet specifies its PCI bus clock operating range to be 20MHz to 33MHz (Data Sheet page 2 and page 7).

Problem

When the 21140A is operated at a PCI clock frequency below 24.9MHz, it is possible that a CRC error may occur on the transmission of a packet at a 100Mbps data rate. This anomaly does not occur at the common PCI operating frequencies of 25MHz, 30MHz or 33MHz.

Implications

The 21140A may not function properly if the PCI bus is operated at a frequency slower than 24.9MHz.

Workaround

No workaround is necessary if the system PCI frequency is 24.9MHz or higher. If the PCI frequency is lower than 24.9MHz, reliability of the 100Mbps data transmissions cannot be guaranteed.

8.2. Receive All Address Recognition Mode

Background

The 21140A Hardware Reference Manual specifies a Receive All address recognition mode, enabled by setting CSR6<30>=1. In this mode, the 21140A processes all incoming packets regardless of the destination address. After address filtering, if the destination address matched the 21140A, the address match status is reported by clearing the Filtering Fail status bit of the receive descriptor (RDES0<30>).

Problem

If the 21140A is operated with Receive All mode enabled (CSR6<30>=1) and Pass Bad Frames disabled (CSR6<3>=0), and the 21140A receives a runt frame which has a valid address match, the 21140A will clear RDES0<30> (this indicates a successful address match). Because Pass Bad Frames is disabled, the 21140A discards this packet. However, the 21140A does not reset the Filtering Fail status bit in RDES0, and during the subsequent frame an address match will be reported even if that frame's destination was not the 21140A.

Implications

The 21140A may identify frames with unmatched addresses as matched frames in RDES0.

Workaround

This issue can be worked around in software by enabling the Pass Bad Frames bit (CSR6<3>=1) whenever Receive All mode is enabled (CSR6<30>=1). With both modes enabled, the 21140A will receive all runt frames. Filtering of the runt frames can then be performed by the driver. Using this workaround, the status of address filtering in RDES0<30> is always correct.

8.3. Initialization of Promiscuous Mode

Background

The 21140A Hardware Reference Manual specifies in Table 3-40 that Promiscuous Mode (CSR6<6>) is enabled following power-up. Also, in Table 3-45, it indicates that CSR6<6> is set following reset.

Problem

The state of Promiscuous Mode (CSR6<6>) is indeterminate following power-up and is unaffected by hardware reset.

Implications

The status of the 21140A's Promiscuous Mode is unknown until CSR6 has been initialized.

Workaround

Software for the 21140A must initialize CSR6 following reset.

8.4. Operating Voltage Range

Background

The 21140A Data Sheet specifies in Table 10 that the power supply voltage and vdd_clamp operating ranges are rated from minimum +3.0V to maximum +3.6V.

Problem

At this time, the power supply voltage and vdd_clamp operating ranges which can be guaranteed for the 21140A are minimum +3.135V to maximum +3.465V. The vdd_clamp specification for 5.0V PCI signaling environments is unaffected.

Implications

All timing and DC specifications for the 21140A are guaranteed across the device's operating voltage range. Therefore, the 21140A's timing and DC specifications are not guaranteed outside of the range from +3.135V to +3.465V.

Workaround

This item does not have a workaround.

8.5. Receive Process Behavior Following an Overflow

Background

A detailed description of the 21140A's receive operation is described in Section 4.3.5 of the 21140A Hardware Reference Manual.

Problem

There is an anomaly in the 21140A receive machine that may occur during the processing of an overflow. This situation has been observed only during heavy receive stress testing and is most likely to occur when the 21140A has poor write access to memory through the host bridge.

Implication

The 21140A's receive process could hang following the occurrence of a receive overflow. It is also possible that invalid data could be transferred to memory without an error indication following an overflow.

A software workaround for the 21140A is available that completely avoids the potential hang situation and prevents the invalid data transfer. For users of drivers developed by DIGITAL Semiconductor, this workaround has been implemented beginning with the indicated driver revisions:

Novell ODI server version 2.10
Novell ODI client version 2.33
NDIS2 version 2.30
NDIS3 version 4.02
SCO UNIX version 3.20

For applications using drivers not developed by DIGITAL Semiconductor, it will be necessary to implement the software workaround.

Workaround

General Description

The workaround relies on the fact that whenever the anomaly occurs, the receive overflow counter always indicates that an overflow has occurred. The overflow does not necessarily imply that a hang will occur; however, each overflow should be treated as a potential occurrence. Stopping the receive process, then restarting it, resolves the hang.

Since there is also a possibility that invalid data has been transferred into host memory without an error indication, all pending frames currently queued into the receiving descriptor must be discarded prior to restarting the receiver.

Although this workaround can cause packets to be discarded, it has negligible impact on performance because the 21140A experiences very few, if any, receive overflows in most PCI implementations. In these systems, the core of the workaround is rarely, or never, executed. Even in a system with poor PCI throughput, the performance of the 21140A is limited by the PCI throughput and not by the overhead of the software workaround.

Detailed Algorithm

At the beginning of the routine that processes receive frames:

1. Verify that the revision of the 21140A requires the workaround (this errata is only for 21140A revisions that identify themselves as CFRV<7:0>=20(hex) and CFRV<7:0>=21(hex)).
2. If the workaround is required, then mark all pending frames that are currently queued into the receive descriptor ring.
3. If one or more overflows have been indicated in the Overflow Counter CSR8<OC> since the last time receive frames were processed:
   A. Stop the Receive process (CSR6<SR>=0).
   B. Poll the Receive Process State (CSR5<RS>) until it indicates that the Receive process has stopped (the receiver will either stop immediately if no reception is in progress, or upon the completion of the present data transfer to host memory if a reception is in progress).
   C. Discard all marked and unmarked pending frames that are queued in the Receive descriptors (do not indicate these frames to the upper protocol levels).
   D. Point to the next descriptor owned by the adapter.
   E. Increment any operating-system required statistic counters to indicate the total number of discarded frames.
   F. Restart the Receive process (CSR6<SR>=1).
4. If no overflows have occurred since the last time receive frames were processed:
   A. Process only the marked frames that have been queued.
   B. If the Receive queue is not empty (new frames have been queued), repeat the sequence from Step 1.

9.0 Controller Connector Pin-Out

To fit within the low profile of the PMC bulkhead the DE520 uses a low profile RJ-45 connector. The table below lists the pin assignments for the connector. Figure 1 shows the rotation of the pin assignments on the mating plug.

Pin Number	**Wire Color**	**Signal Name**
1	White/Green	Transmit +
2	Green/White	Transmit -
3	White/Orange	Receive +
4	Blue/White	NC (No Connection)
5	White/Blue	NC
6	Orange/White	Receive -
7	White/Brown	NC
8	Brown/White	NC

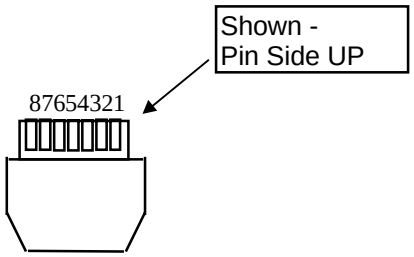

FIGURE 1

10.0 Adapter Cable

To connect the DE520 to a standard RJ-45 connector use the transition adapter cable supplied with the controller or use the following information to build your own. The transition adapter cable is a straight through, "one to one" (NO crossover), connection.

Low Profile RJ-45 Plug (Controller End) -

Stewart Connector Systems, Inc.
Compu-shield connector
Part Number SS-310808-5

Tools Required - Hand Tool - p/n 2940231-01 with .235 inch ferrule - p/n 2912512-01 and Series 31 8-Pin Die Set - p/n 2907502-01.

RJ-45 Receptacle, Cable Mount (Panel Mount) -

Stewart Connector Systems, Inc.
Part number SS-800810-040-250

Tool Required - Arbor Press

Wire List -

Plug End Pin Number	**Wire Color**	**Signal Name**	**Receptacle End Pin Number**
1	White/Green	Transmit +	1
2	Green/White	Transmit -	2
3	White/Orange	Receive +	3
4	Blue/White	NC (No Connection)	4
5	White/Blue	NC	5
6	Orange/White	Receive -	6
7	White/Brown	NC	7
8	Brown/White	NC	8

11.0 Loopback Connector

A loopback connector can be constructed with a plug by connecting the following pins:

Wire List -

Pin Number	**Signal Name**	**Pin Number**	**Signal Name**
1	Transmit +	3	Receive +
2	Transmit -	6	Receive -

12.0 DE520 PMC Fast Ethernet Board Schematics

Schematics are available by special arrangement under a non-disclosure agreement.